Monolithic FET Structures for High-Power Control Component Applications

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Abstract—**A new monolithic switch FET control circuit has been developed that can be integrated with other monolithic functions or used as a discrete component in an MIC structure. This device increases the power-handling capability of the conventional single FET switch by an order of magnitude. It does this by overcoming the breakdown voltage limitation of the FET device. The design, fabrication, and performance of two high-power control components using these circuits are described as examples of the implementation of this technology (an L-band terminated single-pole single throw (SPST) switch and an L-band limiter).**

I. Introduction

THIS PAPER describes the use of GaAs MMIC technology in high-power (10 to 100 W range) signal control applications. The microwave signal switching component which is still in common use today is the silicon p-i-n diode. However, the GaAs switch FET is finding quick acceptance as a p-i-n diode replacement in several applications, the advantages being fast switching speeds, simplified bias networks, monolithic compatibility, and lower power consumption driver circuitry. GaAs switch FET technology has been demonstrated over wide bandwidths at low power levels (20 dBm) [1]. Higher power levels have been attained by using impedance transformation; this technique places the switch FET at a lower impedance point and thus reduces the voltage stress on the device. By means of this technique, 10 W switches have been demonstrated by transforming from 50 to 18 Ω [2]; however, due to the required impedance transformation, the approach is applicable over a limited frequency bandwidth. The FET circuit discussed in this paper is a suitable replacement for p-i-n diodes as a generic control element in applications from ten watt to several hundred watt CW, and has all the fundamental advantages of the GaAs FET. Two control functions implemented with this circuit configuration are presented as examples of its utility as a high-power p-i-n diode replacement.

II. FET Circuit Description

The power performance of an FET is limited by its current-handling capability in its low-impedance state and by its breakdown voltage in its high-impedance state. The current handling of an FET can be increased by increasing its periphery. To understand the benefits of the monolithic switch circuit described in this paper, the voltage limitations of an FET in the switch mode need to be studied in detail. The variation of the RF voltage on the drain and gate terminals with respect to the grounded source is shown in Fig. 1 for one period [2]. In this figure, it is assumed that the gate terminal of the FET is an RF open. This condition should be realized in the design of the gate bias circuitry.

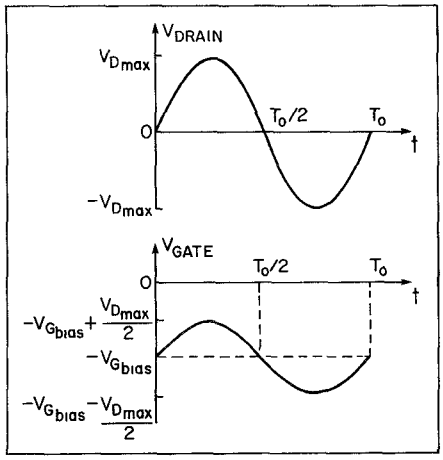

Fig. 1. Variation of the large-signal RF voltages on the drain and gate terminals over one period.

Under the above assumption and because gate-to-drain impedance and gate-to-source impedance are equal, half of the drain voltage swing appears in the gate termination, as illustrated in Fig. 1. Constraints on the terminal voltages can be summarized as follows. During the first half of the period, the total gate voltage should not fall below the pinch-off voltage V_p. During the entire cycle, the difference between the drain and gate voltages should not exceed the gate drain breakdown voltage V_B. These constraints can be expressed mathematically as

$$-V_{G\,\mathrm{bias}} + V_{D\,\mathrm{max}}/2 = -V_p \tag{1}$$

and

$$V_{D\,\mathrm{max}} + V_{G\,\mathrm{bias}} - V_{D\,\mathrm{max}}/2 = V_B. \tag{2}$$

From these two equations, the maximum allowable drain voltage and the required gate bias condition can be solved as

$$V_{D\,\mathrm{max}} = V_B - V_p \tag{3}$$

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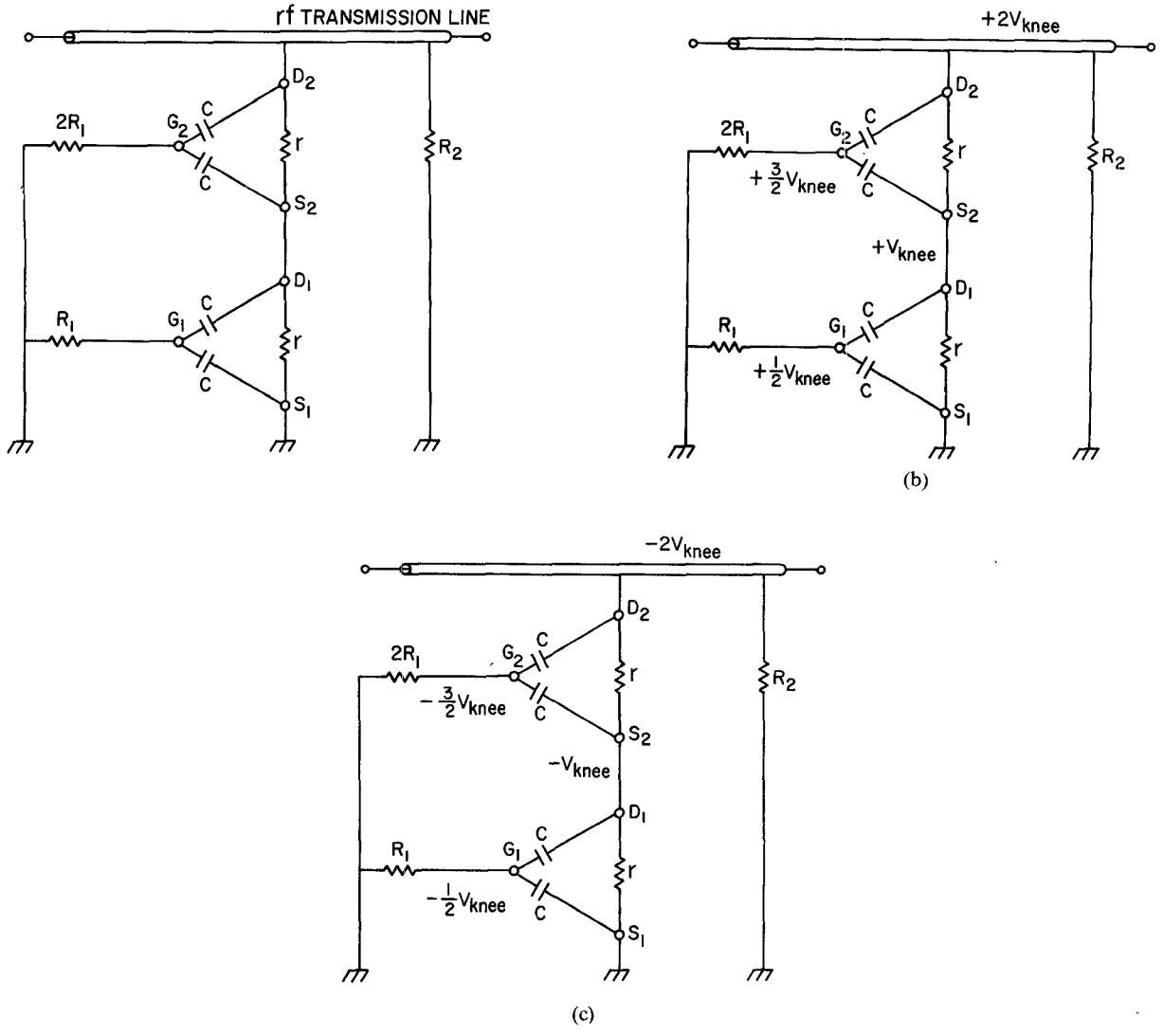


Fig. 2. Low-impedance equivalent circuit under small- and large-signal conditions. (a) Small signal with no significant RF voltage. (b) Large signal, at maximum positive voltage peak. (c) Large signal, at maximum negative voltage peak.

and:

$$V_{G\,\text{bias}} = (V_B + V_p)/2. \tag{4}$$

Hence, if the FET is shunt mounted in a system with Z_0 characteristic impedance and the FET is in its high-impedance state, the maximum power that it transfers can be calculated as

$$P_{\max} = (V_B - V_p)^2/2Z_0. \tag{5}$$

$V_{D\max}$ ranges between 10 and 18 V for most GaAs foundries. This corresponds to a range of 1 to 3.25 W in a 50 Ω system. Since p-i-n diodes have breakdown voltages five to ten times higher than FET's, they can control much higher power. Thus, to achieve the benefits of GaAs switch FET technology at high power levels, a new approach that is capable of controlling larger voltage swings is required. The new monolithic switch structure has been developed to meet this requirement.

The new circuit configuration allows a number of FET cells to be connected in series. In describing the operating principle, a two-cell FET will be considered in the following analysis. The conclusions, however, are applicable to an arbitrary number of cells, in shunt or series with the RF transmission line.

Let us first consider the low-impedance state, which means no dc voltage is applied to the device gate terminal with respect to its drain and source terminals. The FET's are represented in Fig. 2(a) by their equivalent circuits. Under small-signal operation, both devices have negligible voltage applied to their source–gate junction; therefore both channels are effectively under zero bias condition. Now consider large-signal operation; the largest voltage that can be handled in the linear region in this low-impedance state is $\pm 2V_{\text{knee}}$. For typical V_{knee} voltages of 1.5 V, this translates to ± 3 V.

Fig. 2(b) shows the voltage distribution during the positive peak. Note that V_{G1} is $\frac{1}{2}V_{\text{knee}} = 0.75$ V, positive with respect to V_{s2}. This small positive voltage can be handled by the gate junction and, in fact, will help reduce the low field resistance, r, somewhat by fully opening the channel under the gate. The same argument applies to V_{G2}.

During the negative peak, the voltages are as shown in Fig. 2(c). V_{G2} is now more negative then V_{s2}, but this does not pinch off the channel conduction because V_{D2} is the

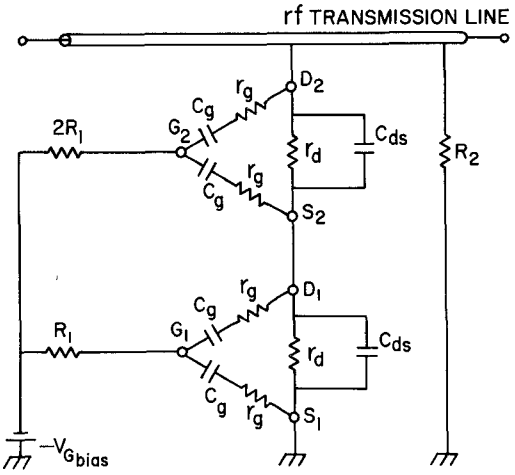


Fig. 3. High-impedance-state equivalent circuit.

most negative point. Therefore, the D2–G2 junction is now +0.75 V positive biased, still giving the benefit of a fully open channel. The same argument applies to the D1–G1 junction.

Now let us consider the high-impedance state, where the gate terminals are biased at

$$V_G = -V_{G\,\text{bais}} = -(V_B + V_p)/2. \tag{6}$$

Fig. 3 shows the equivalent circuit for this state. Assuming a large-signal RF voltage on the transmission line, with peak voltage of $\pm V_{\max}$, the potential variations over one period with respect to ground are plotted in Fig. 4. We have also assumed that the gate terminals are RF open ($R_1 \gg 1/4\pi f C_{gs}$). R_2 is also a high value resistor to be considered an RF open; it is there to provide dc continuity. It can be eliminated if impedance matching circuitry provides a dc path.

The voltage levels in Fig. 4 indicate that the first FET behaves like the single FET described in Fig. 1, with the ability to handle a maximum peak-to-peak voltage of $V_B - V_p$. This is contingent upon the second FET's staying in the pinched-off high-impedance state during the full RF cycle. We note in Fig. 4(b) that, in fact, the voltage on the second gate goes well into the positive region. However, it is positive with respect to ground and not with respect to its source terminal S2. To show that more clearly, the source voltage S2 is subtracted from $V_{D2}(t)$ and $V_{G2}(t)$ and the resultant signal voltage is superimposed in the same figure. These dotted curves are now not very different from $V_{D1}(t)$ and $V_{G1}(t)$. Hence the conditions derived in (1) to (5) apply equally well to the second FET.

The important conclusion is that if each FET can handle $V_B - V_p$ between their drain to source terminals, then two of them connected in the proposed configuration can handle $2(V_B - V_p)$. Thus maximum power switching capability due to the breakdown voltage limitation has been increased by a factor of 4.

The switch circuit design starts with the power control requirements. This establishes the number of series FET cells, and the periphery of each of these cells. The equations are given by

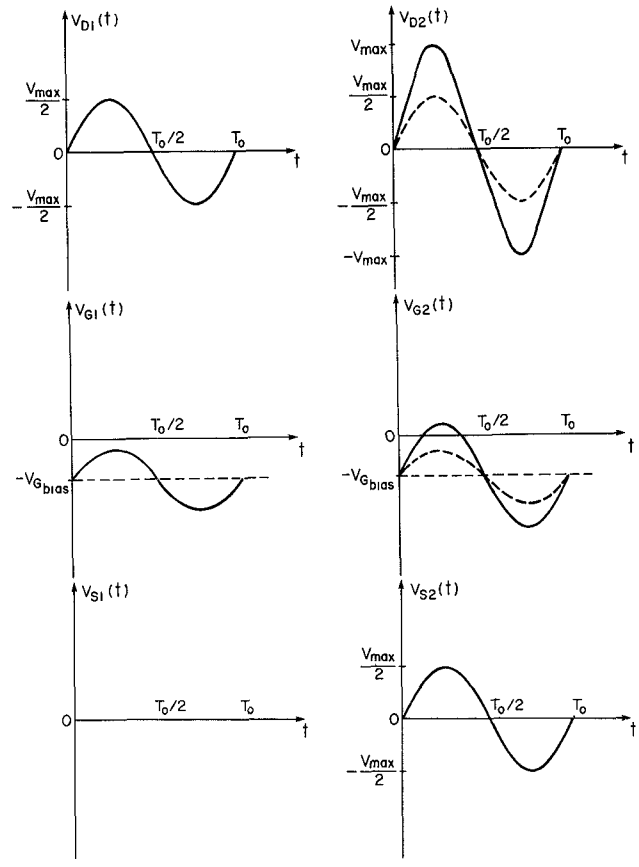


Fig. 4. Relative levels of RF voltage variation at six device terminals during a full RF swing. All voltages are with respect to ground except the dotted curves, which are with respect to VS2.

$$N = V_{\text{pk}}/V_{D\max} \tag{7}$$

$$w = I_{\text{pk}}/I_{DSS} \tag{8}$$

where I_{DSS} is the saturation current of the FET, typically expressed in terms of current per unit length, N represents the number of FET cells required, V_{pk} and I_{pk} are the peak RF voltage and current respectively, and w is the FET cell periphery.

III. Bias Network Considerations

The bias network establishes four important operating characteristics of the monolithic switch circuit: the switching speed, the cutoff frequency, the loss in the bias circuit, and the uniform RF voltage distribution required during switching transients. There are many possible bias circuit topologies. The choice of a particular bias network topology is influenced by the above specifications and by power handling requirements, available bias supplies, switch circuit configuration, and monolithic fabrication issues, such as chip size and yield. The circuits fabricated for the applications in this paper have been designed with a resistive bias topology. Monolithic resistors are high yield and compact, allowing the bias network to be located on the chip. In this topology each FET cell has a resistor connected between its gate and the common bias supply as shown in Fig. 5. The resistor value is the same for each cell

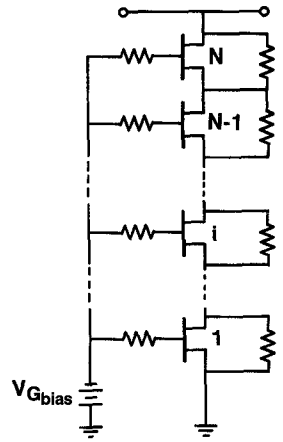


Fig. 5. Schematic of a resistor bias network used to fabricate the monolithic switch circuits described in this paper.

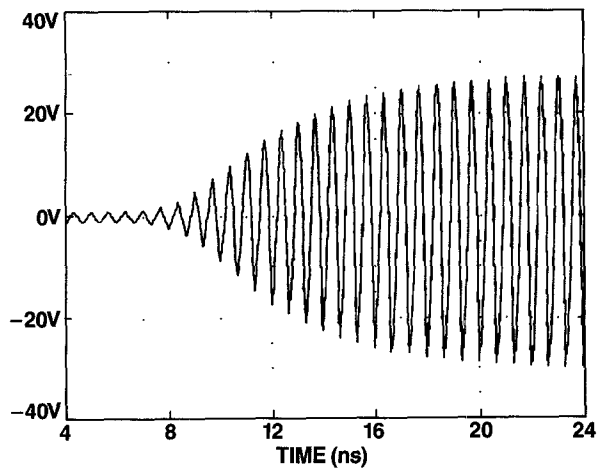


Fig. 6. This figure shows the drain–source voltage for each FET cell in a four-cell stack. The switching transient switches the stack from its low-impedance to its high-impedance state. The voltages remain balanced to within 1 V throughout the entire transition.

in the stack. As the switching time τ for each cell is given by

$$\tau = RC_{ge} \tag{9}$$

where C_{ge} is the effective gate capacitance for each cell, all the FET's in the stack will switch simultaneously. Large-signal SPICE simulations of a four-cell circuit with this bias circuit topology have been conducted. Fig. 6 shows the result for the switching transient of a four-cell stack. It can be seen that the drain–source RF voltage swings across the individual FET cells remain within 1 V of each other even during the transient. Having established that this is a viable bias topology, issues that influence the selection of the resistor value R need to be considered.

The value selected for the gate resistor R determines a low-frequency cutoff, below which the monolithic switch circuits' power handling will decrease. This degradation can be explained by considering a resistor biased single FET mounted with its source grounded and drain connect to the RF line. In its "off" state the gate capacitance forms a voltage divider with half the capacitance between the gate and the drain, and the other half between the gate and the source. Therefore, as described in the previous section the RF line voltage swing divides equally between the drain and gate, and the gate and source. However, at lower frequency the voltage no longer divides equally since the gate resistor appears in shunt with that half of the gate capacitance between the gate and source. Thus, more of the voltage is dropped between the drain and the gate. In fact, at very low frequencies all the drain voltage is dropped across the drain and gate terminals. For a single FET the peak drain–gate (V_{dg}) and drain–source (V_d) RF voltage swing are related as

$$V_{dg} = V_d\sqrt{(1+X^2)/(1+4X^2)} \tag{10}$$

$$X = 2\pi f C R_s \tag{11}$$

where f is the RF signal frequency, R_s is the gate resistor value, and C is half the total gate capacitance of the FET in the pinched-off state. V_{dg} cannot exceed the breakdown-limited value of $(V_B - V_p)/2$, where V_B and V_p are the FET breakdown and pinch-off voltages, respectively. Hence, for a finite fR_s product, the maximum drain–source voltage swing ($V_{D\max R}$) has to be reduced below the ideal $V_{D\max}$ value defined in (3). For a given $V_{D\max}$ derating factor k, R_s is given by

$$R_s = (1/2\pi f C)\sqrt{(1-4k^2)/4(k^2-1)} \tag{12}$$

where

$$k = V_{D\max R}/V_{D\max}. \tag{13}$$

This translates to a corresponding reduction in the FET's power handling capability, compared to that achievable with an infinite gate bias network impedance. The minimum value for the gate resistors in the FET stack, for a given voltage derating factor and operating frequency, can be derived from the single FET value as

$$R > ((2N-1)Rs)/N \tag{14}$$

where N is the number of FET's in the stack. Equation (14) assumes that the periphery of each FET in the stack increases linearly with N, so as to maintain the characteristic impedance of the circuit as its power handling capability is increased. Using (9), the minimum R_s switching time for the stack is derived as

$$\tau_{\min} = R_s(2N-1)C_{ge} \tag{15}$$

where C_{ge} is the effective gate capacitance of the single FET switch.

While the minimum resistor value given by (14) may be acceptable from the point of view of the peak RF voltage swing across the FET cells, it could lead to excessive RF power loss in the bias network. This loss is given by

$$P_{\text{dis}}/P = Z_0(1.33N^2 - 0.33)/(2N-1)4R_s \tag{16}$$

Where P_{dis}/P is the ratio of the dissipated power in the bias network to the total power being controlled. This ratio increases approximately linearly with N. The bias network power dissipation can be reduced by using larger resistor values, but the switching speed will decrease accordingly.

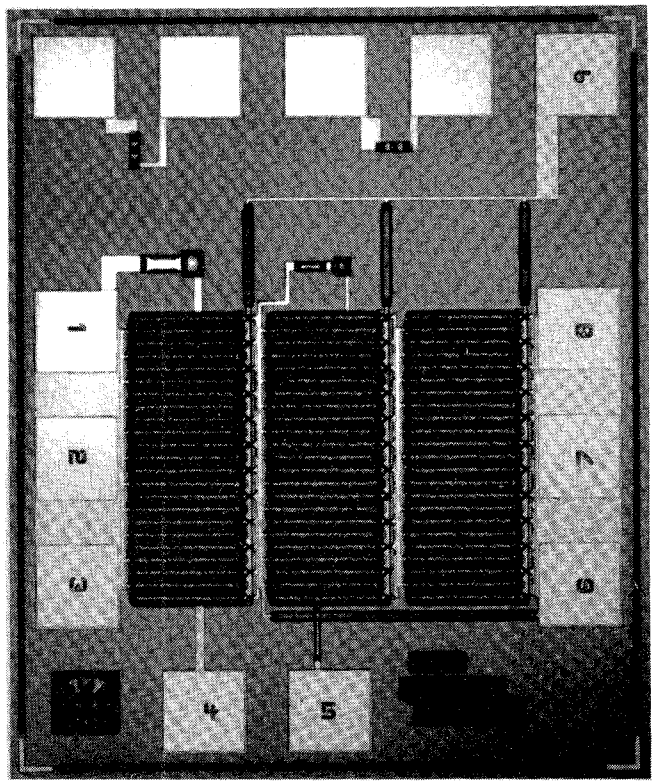


Fig. 7. Photograph of a three-cell switch circuit.

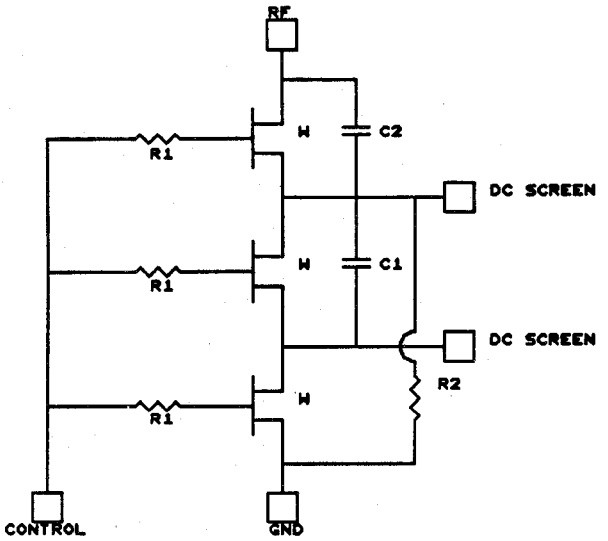


Fig. 8. Schematic of the three-cell circuit shown in Fig. 7.

IV. Parasitic Capacitance Considerations

Fig. 7 shows an example of a series switch circuit. The schematic of this chip is provided in Fig. 8. The core of the circuit design comprises the three series-connected FET's, all with periphery w. Additional elements are incorporated in the circuit design to achieve an even voltage distribution across the series-connected FET's. The monolithic chips were mounted in a microstrip hybrid circuit. The individual FET's in the stack have a parasitic capacitance to the ground plane through the GaAs chip substrate. This parasitic causes a nonuniform voltage distribution across the FET's in the stack. The two capacitors in the schematic in Fig. 8 have been added to compensate for this effect. For a stack of N FET's, there are $N-1$ capacitors and their values can be determined by the following equation:

$$C_i = i(i-1)C_p/2 \tag{17}$$

where C_p is the parasitic capacitance, and C_i is the compensation capacitor connected across the ith FET from the ground end of the stack.

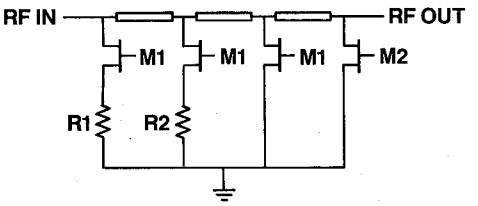
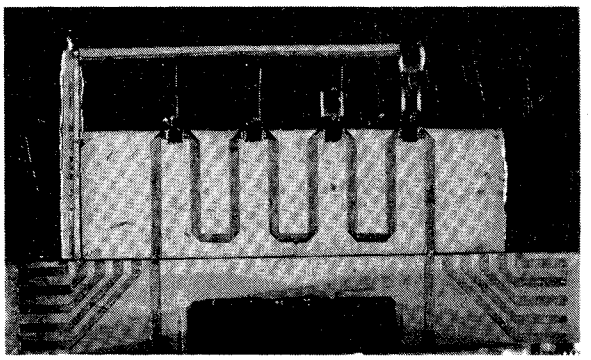


Fig. 9. Circuit topology used for the matched SPST switch.



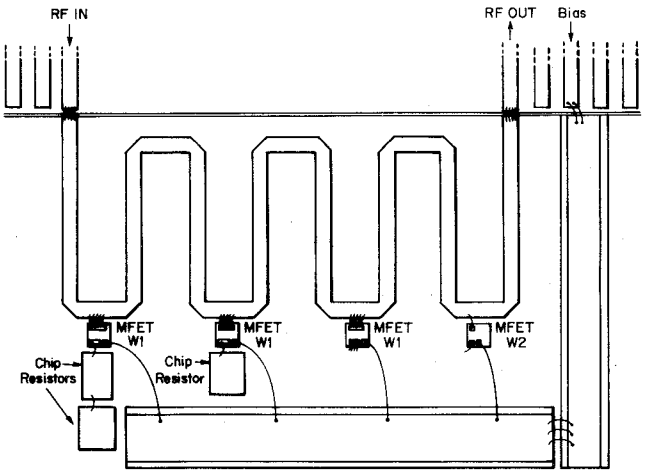


Fig. 10. Picture and drawing of a terminated high-power SPST switch.

V. Device Performance

The demonstration device shown in Fig. 7 has been tested to 27 W (the limit of our signal power source), corresponding to 52 V peak RF voltage, in a 50 Ω system. However, the device did show signs of insertion loss compression at 21 W, corresponding to 45 V RF. Thus, each FET cell in this particular process is capable of controlling 15 V.

A four-cell device has also been fabricated. Based on the three-cell results, its power control capability in 50 Ω is

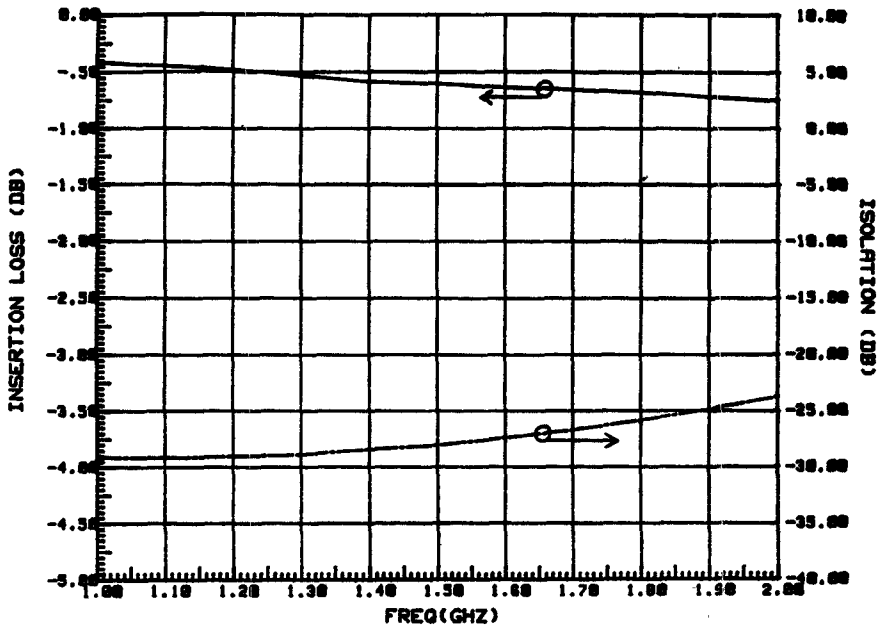


Fig. 11. Measured insertion loss and isolation of a matched SPST switch, fabricated with four-cell monolithic switch circuit.

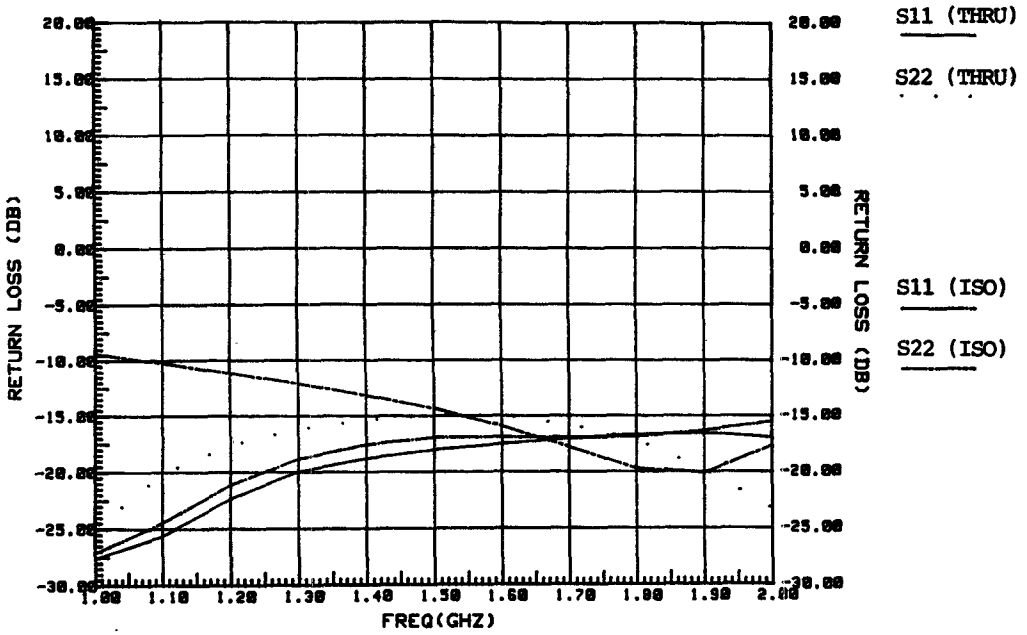


Fig. 12. Measured return loss performance of a SPST switch in both states, fabricated with four-cell monolithic switch circuits.

expected to be 40 W. This device was tested up to 27 W with no sign of compression.

These circuits are used in the same fashion as an FET switch with gate bias resistors already integrated. Both of these circuits have been used in the fabrication of the control functions described in this paper.

VI. *L*-Band Terminated SPST

This SPST switch is designed to operate at 1.5 GHz with an octave bandwidth. The SPST is an all-shunt design, as shown in the schematic in Fig. 9. The switch is asymmetric in that there is a high-power port (RFIN), and a low-power port (RFOUT). The RFOUT port is shunted by a monolithic switch circuit, designated M2. This circuit is sized to provide a low-power match to the output when the switch is in the isolation state. The monolithic switch circuits labeled M1 are much larger in periphery since they must cope with a higher current level than M2. This switch is an absorptive switch and therefore must dissipate the incident RF power when the switch is in the isolation state. The resistors labeled R1 and R2 are high-power chip resistors sized to handle the RF power dissipation. Their values were designed to provide a good match over the band and to balance the current evenly between the M1 elements. The switch was fabricated using microstrip transmission lines, as shown in Fig. 10.

Fig. 11 shows the measured insertion loss and isolation on a 40 W version of the terminated switch topology. This switch was fabricated with four-cell devices. The insertion loss is a maximum of 0.75 dB across the band, and the

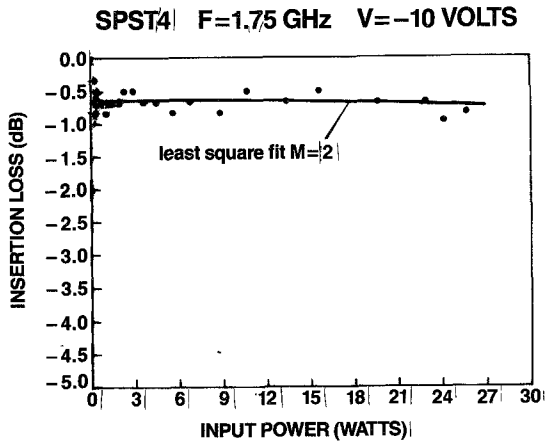


Fig. 13. Measured insertion loss versus input power for a SPST switch fabricated with a four-cell monolithic switch circuit.

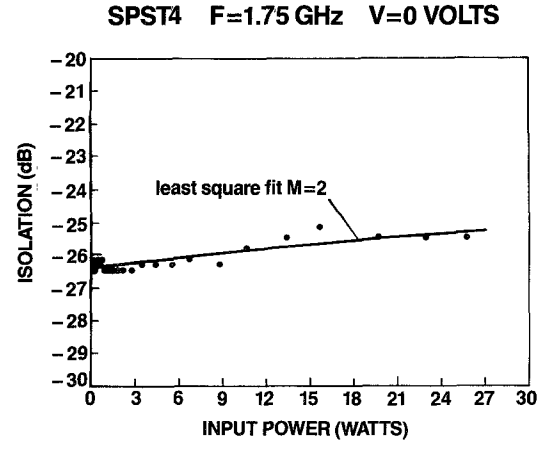


Fig. 14. Measured isolation versus input power for a SPST switch fabricated with a four-cell monolithic switch circuit.

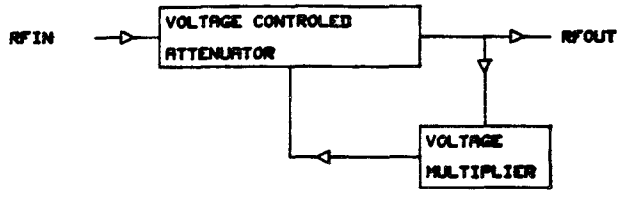


Fig. 15. Block diagram for the limiter.

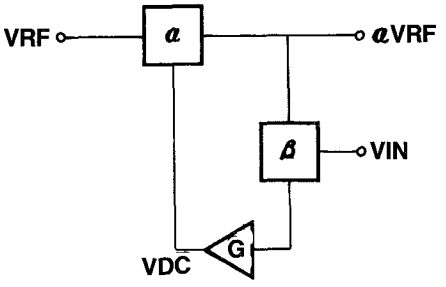


Fig. 16. Limiter feedback analysis block diagram.

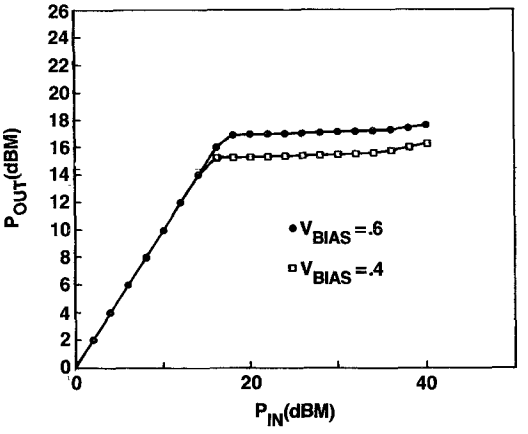


Fig. 17. Limiter simulation results.

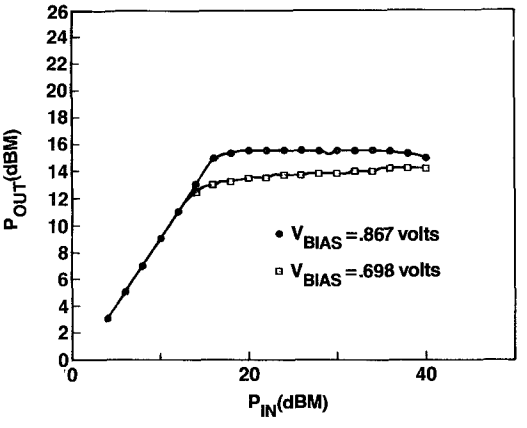


Fig. 18. Measured performance of the limiter.

isolation is a minimum of 24 dB. Fig. 12 shows the switch return loss at both ports in both states. The return loss at both ports was equal to or better than 15 dB across the band in the transmission state. For the isolation state, the output return loss decreased to 9 dB at 1 GHz.

Figs. 13 and 14 show the power performance of the SPST fabricated with four-cell devices. The switch was tested and did not expand (out of isolation) or compress (out of insertion loss) up to 27 W (the limit of the TWTA that was available for measurements).

VII. *L*-Band Limiter

A block diagram of the limiter is shown in Fig. 15. The limiter is composed of two components; a voltage-controlled attenuator (VCA) and a voltage multiplier (VM) amplitude detector circuit. In operation, the VM detects the RF amplitude of the output of this attenuator. The dc voltage of the output of the VM is fed back to the control input of the attenuator so as to increase the attenuation level as the RF input level increases. A fixed dc bias is superimposed on the output of the detector to adjust the limiting threshold. Fig. 16 shows the feedback network used to simulate the limiter. The loop equation is given by

$$VDC = G(V_{\text{in}} - \alpha\beta VRF) \tag{18}$$

where G is the gain of the amplifier, V_{in} is the dc bias voltage, VRF is the peak RF line voltage, α is the level of attenuation in the switch, β is the multiplication factor of the voltage multiplier, and VDC is the voltage at the control port of the attenuator.

The SPST switch described in the previous section was designed to provide low return loss even at intermediate

gate control voltages between transmission and isolation. It is thus ideally suited for use as a voltage-controlled attenuator. The attenuation of the SPST is dependent on *VDC*. A function modeling this dependence has been derived. This function, along with (18), can be used to simulate the limiter performance. Fig. 17 shows the results of this simulation. The limiter simulation has a flat limiting response with an adjustable limiting threshold.

A doubler circuit [3] was used for the voltage multiplier. A voltage doubler ideally provides a rectified dc voltage that is twice the peak ac line voltage. However, it was found that output loading and diode and substrate parasitics reduced the output voltage from this circuit to approximately 40 percent of the peak RF voltage on its input. Hence, it was necessary to include an operational amplifier between the detector circuit on the attenuator control input so as to provide enough loop gain. Fig. 18 shows the measured performance of this limiter configuration at two different dc offset bias settings. The limiter was tested at 1.5 GHz and up to a power level of 40 dBm. The limiting range is limited to the attenuation range of the SPST switch, which is 25 dB. Thus, if the limiter cuts in at 15 dBm, then output power will start to increase again at about 40 dBm. It is possible to have limiting action over a wider power range by using a switch with higher isolation. At the lower bias voltage the limiting action starts at a power level of 14 dBm, and at the higher bias voltage the limiter cuts in at 16 dBm. As can be seen these results agree well with the simulated results. The settings of the bias voltages are different by about 0.3 V. This is due to the finite output offset voltage of the operational amplifier used in the limiter circuit.

VIII. Conclusion

GaAs MMIC technology is generally considered to be applicable for small to medium power levels up to the 1 to 2 W range. In this paper, we have presented a monolithic FET circuit which allows the power handling capability of these devices to increase by an order of magnitude or higher. We have demonstrated this concept by using these devices for two different power control functions.

Acknowledgment

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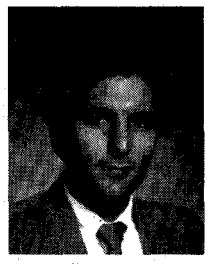

Mitchell B. Shifrin (M'86) received two B.S. degrees from the University of Wisconsin, at Madison in 1980: one in electrical and computer engineering, the other in applied mathematics and engineering physics. In 1980, he received a Raytheon Company Fellowship, which enabled him to attend the University of Massachusetts, where in 1981 he received the M.S. degree in electrical engineering. He concentrated his studies in the areas of solid-state devices and microwave circuits.

After graduating from the University of Massachusetts, he worked for the Raytheon Company in the Special Microwave Device Operation (SMDO). While at SMDO, he was a member of both the multi-function package and the broad-band amplifier group. He was responsible for the design and shipment of MIC assemblies for ECM applications. In 1986, Mr. Shifrin joined the Hittite Microwave Corporation, Woburn, MA, where he is engaged in the design of novel MMIC products.

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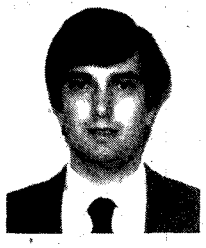

Peter J. Katzin (S'82–M'82) received the B.S. degree in physics and electrical engineering from the University of Manchester, England, in 1979. His graduate study was at Cornell University, where he received the M.Eng. degree in electrical engineering in 1983. As part of his graduate work, he designed, fabricated, and characterized a low-noise *Ku*-band GaAs MESFET amplifier.

From 1980 to 1981, he was with the Space and Communications Division, Hughes Aircraft Company, where he contributed to the design and testing of the attitude control and the microwave command, tracking, and ranging systems of communication satellites. In 1983, he joined the Research Division of the Raytheon Company. There, he participated in the evaluation, design, and CAD modeling of GaAs MMIC components and circuits. He was program manager for a 44 GHz MMIC power amplifier program and a high-efficiency *S*-band MMIC switching power amplifier program. In 1987, he joined the Hittite Microwave Corporation, where he is involved in MMIC design.

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Yalcin Ayasli (M'79–SM'84) holds the Sc.D. degree from Massachusetts Institute of Technology.

He is the founder of Hittite Microwave Corporation, Woburn, MA, which specializes in the development of microwave and millimeter-wave integrated circuit (MMIC) components and subsystems for military and commercial markets. He has been involved in theoretical and experimental studies of microwave monolithic integrated circuit techniques involving GaAs field-effect transistors (FET's) and related devices since 1979. He managed research and development programs at Raytheon Research Division which included circuit design, semiconductor wafer processing, and device measurement and characterization. In this capacity, he was the program manager for several government R&D programs for wide-band amplifiers and transmit/receive modules.

Dr. Ayasli is the author or a number of technical papers and holds several patents related to FET's and their monolithic applications. He was the General Chairman for the 1987 IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium. He was also a corecipient of the 1986 IEEE Microwave Prize for his work on wide-band monolithic traveling wave amplifiers.